



# PRODUCT/PROCESS CHANGE NOTIFICATION

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PCN AMS-AAS/14/8519  
Dated 10 Jun 2014

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**Additional Back End capacity in Nantong Fujitsu for  
Signal conditioning products in TSSOP14 package (Analog  
and Audio Systems Division - AMS Group)**

**Table 1. Change Implementation Schedule**

Forecasted implementation date for change	03-Jun-2014
Forecasted availability date of samples for customer	03-Jun-2014
Forecasted date for <b>STMicroelectronics</b> change Qualification Plan results availability	03-Jun-2014
Estimated date of changed product first shipment	09-Sep-2014

**Table 2. Change Identification**

Product Identification (Product Family/Commercial Product)	Signal conditioning products in TSSOP14 package
Type of change	Package assembly location change
Reason for change	To increase capacity and improve service to ST Customers
Description of the change	Progressing on the activities related to TSSOP14 manufacturing processes expansion, ST is glad to announce an additional production capacity (assembly, test & finishing) for signal conditioning products from Analog and Audio Systems Division (AAS Division) assembled in TSSOP14 package. For reference, production in Nantong Fujitsu for AAS Division is already running since 2008 for signal conditioning products in TSSOP8 and since 2006 for logic products in TSSOP14. For sample requests, please make sure you enter a non-standard sample order with the PCN reference in the comment field.
Change Product Identification	Traceability code (see qualification report section for more information)
Manufacturing Location(s)	

**Table 3. List of Attachments**

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN AMS-AAS/14/8519
Please sign and return to STMicroelectronics Sales Office		Dated 10 Jun 2014
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved  <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name:	
	Title:	
	Company:	
	Date:	
	Signature:	
Remark ..... ..... ..... ..... ..... ..... ..... ..... ..... ..... ..... .....		

## DOCUMENT APPROVAL

Name	Function
Ferri, Simone	Marketing Manager
Onetti, Andrea Mario	Product Manager
Bugnard, Jean-Marc	Q.A. Manager

**PRODUCT/PROCESS  
CHANGE NOTIFICATION**

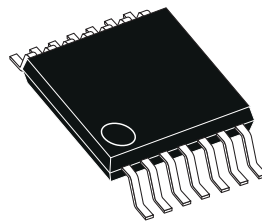
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**PCN AMS-AAS/14/8519**

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## **Analog, MEMS and Sensor Group (AMS)**

**Additional Back End capacity in Nantong Fujitsu for Signal conditioning products  
in TSSOP14 package (Analog and Audio Systems Division)**



**TSSOP14**

**WHAT:**

Progressing on the activities related to TSSOP14 manufacturing processes expansion, ST is glad to announce an additional production capacity (assembly, test & finishing) for signal conditioning products from Analog and Audio Systems Division (AAS Division) assembled in TSSOP14 package. For reference, production in Nantong Fujitsu for AAS Division is already running since 2008 for Signal conditioning products in TSSOP8 and since 2006 for logic products in TSSOP14.

Material	Current process	Modified process
Assembly location	ST Bouskoura (Morocco) / Amkor (Philippines)	Nantong Fujitsu (China)
Die attach	ABLEBOND 8390/ ABLESTICK 8601S25	ABLEBOND 8200T
Wire	Gold 1 mils / copper 1mils	Gold 1mil
Lead frame	Copper	Copper
Molding compound	Shinetsu KMC 184-3 SUMITOMO G630AY	Hitachi CEL9210HFVL
Lead finishing	NiPdAu / NiPdAgAu	Sn

Samples of test vehicles products are available and other products samples will be available upon request.

**WHY:**

To increase capacity and improve service to ST Customers for the affected package.

**HOW:**

The change that covers Signal conditioning products packaged in TSSOP14 is qualified through attached qualification plan. Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.

**WHEN:**

The production for Signal conditioning products is forecasted in July 2014. Production in Nantong Fujitsu for AAS Division is already running since 2008 for Signal conditioning products in TSSOP8 and since 2006 for Logic products in TSSOP14.

**Marking and traceability:**

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled in Nantong Fujitsu will be ensured by marking on package and on label as per below description:

Manufactured under patents or patents pending

STMicroelectronics

Assembled in: **COUNTRY**

PbFree      **Second level interconnect**

MSL: **X**      **Bag sealed date: XX XXX XXXX**

PBT: **XXX°C**      Category: **ECOPACK/Rohs**

**TYPE**      **Commercial product**

**Finished good**

**Total Qty: XXXX**

**Trace codes** **PPYWWLLL WX TF**

**PPYWWLLL WX TF**

**PPYWWLLL WX TF**

**Marking MARKING**

**Bulk Id Number**

Bar code

Please provide the bulk Id for any inquiry

PP and TF code will change from CZ to GU

MSL: Moisture sensitivity level as per Jedec J–std-020C  
 PBT: Peak body temperature (maximum temperature for reflow soldering)  
 ECOPACK: present if leadfree component  
 TYPE: product name  
 Trace codes: PP: assembly plant code  
                  Y: last digit of the year of assembly  
                  WW: Week of assembly  
                  LL1: lot number  
                  WX: Diffusion plant code  
                  TF : Test&finishing plant code

Bulk ID number: 1: Product level (T for tested product)  
                  Y: last digit of the year  
                  P: Plant code  
                  WW: Week of labeling  
                  LOT: Sequential number for lot  
                  BOXX: Sequential number for box

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets. There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).  
In any case, first shipments may start earlier with customer's written agreement.



## Qualification Report

General Information	
Product Line	: 0339, 0464
Product Description	: Quad op amps
Commercial Product	: LM339PT, TS974IPT
Product division/BU	: Analog and Audio system
Package	: TSSOP14
Technology process	: Bipolar, HF2CMOS
Jedec MSL	: 1

Locations	
Wafer fab location	Ang Mo Kio (singapore) Catania (Italy)
EWS plant location	Toa Payoh (singapore) Catania (Italy)
Final test plant location:	Nantong fujitsu (China)

### DOCUMENT APPROVAL LIST

NAME	FUNCTION	DATE	VISA
Jean-Marc Bugnard	Quality Manager AMS Grenoble	28 <sup>th</sup> April 2014	

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.  
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## **1 RELIABILITY and qualification evaluation overview**

### **1.1 Objectives**

The aim of this report is to present the qualification plan of the reliability evaluations performed on LM339PT and TS974IPT (test vehicles) to qualify the production of TSSOP14 package produced in Nantong Fujitsu for Signal conditioning products (AAS Division).

These results will come in addition to the TSSOP8 signal conditioning and TSSOP14 Logic results as they have been qualified previously (PCN 2242 and 7092)

### **1.2 Conclusion**

All results are inside ST specification and the plan to achieve qualification exercise is described in below sections.

TSSOP14 is already produced in Nantong Fujitsu since 2006 for Logic products which also belong to the Analog and Audio Systems Division (AAS). The aim of this document is to explain the additional qualification tests performed to add the production of signal conditioning products in TSSOP14 in Nantong Fujitsu.

## 2 DEVICES TRACABILITY

### 2.1 Wafer fabrication information

	TV1	TV2
Line	0339	0464
Wafer Fab location	Singapore	Singapore
FE process	Bipolar	HF2CMOS
Die size (µm)	1100x1090	1450x1410
Die thickness (µm)	280	280
Metallization	AlSiCu	AlSiCu
Passivation	Si N	Si N+PSG
Back side	Raw Silicon	Raw Silicon

### 3.1 Test vehicle

Lot#	Process/ Package	Product Line	Comments
1	Bipolar / TSSOP14	0339	
2	HF2CMOS / TSSOP14	0464	

Detailed results in below chapter will refer to P/N and Lot #.

### 3.2 Test plan and results summary

Tests	Conditions	Step	TV1	TV2		Comments
		Line	0339	0464		
<b>Die oriented tests</b>						
HTB	Tj=125°C Vs=absolute max rating JESD22 A-108	500h	Ta=125 77	Ta=125		
<b>Package oriented tests</b>						
AC	Ta=121C P=2atm JESD22 A-102	96h	77	77		
TMC	Ta=-65/+150C JESD22 A-104	100cy 500cy	77 77	77 77		
MSL	Baking (150°C) Moisture soak 3 IR reflow soldering	24h MSL1	22	22		

For reference, below results described the tests done previously for TSSOP8 signal conditioning qualification :

Tests	Conditions	Step	TV1	TV2	TV3	Comments
		Line	0158	393	P2VA	
ESD	CDM		0/3	0/3	0/3	
<b>Die oriented tests</b>						
HTB	Tj=125°C Vs=absolute max rating JESD22 A-108		Ta=125	Ta=125	Ta=150	
		168h	0/78	0/78		
		1000h	0/78	0/78		
<b>Package oriented tests</b>						
THB	Ta=85C RH=85% Vs=nominal JESD22 A-101	168h	0/78	0/78	0/24	
		1000h	0/78	0/78	0/24	
AC	Ta=121C P=2atm JESD22 A-102	168h	0/78	0/78		
		240h	0/78	0/78		
Env seq	TMC + AC	100cy			0/50	
		168h			0/50	
TMC	Ta=-65/+150C JESD22 A-104	100cy	0/78	0/78	0/50	
		500cy	0/78	0/78	0/50	
		1000cy	0/78	0/78		
MSL	Baking (150°C) Moisture soak 3 IR reflow soldering	24h	0/22	0/22	0/5	MSL 1 passed
		Jedec	0/22	0/22	0/5	
		260°C	0/22	0/22	0/5	

For reference, the below results described the tests done previously for TSSOP14 Logic qualification :

MPA (Micro, Power, Analog) Group  
Voltage Regulator, Interface, Advanced logic & Power RF  
Quality & Reliability

REL-019W06

Reliability Evaluation Plan and Results on  
**NANTONG FUJITSU – TSSOP Package**

Test	Conditions	S.S.	Requirement	Results
PRECONDITIONING OF SMD DEVICES BEFORE TC/THB/PP	DRYNG 24H @ 125°C STORE 192H @ TA=30°C RH=60% IR 3 times @ Tmax= 260°C		Parameter deviation within spec. limits at end of preconditioning - go no go	No parameter deviation out of spec. limits at end of preconditioning
H.T.S.	TA=150°C	77x3 Lot	Parameter deviation within spec. limits at 1000h	No parameter deviation out of spec. limits at 1000 hours
T.H.B.	<i>D.U.T. PRECONDITIONED</i> TA=85°C – RH=85% Vbias	77x3 Lot	Parameter deviation within spec. limits at 1000h	No parameter deviation out of spec. limits at 1000 hours
H.T.B.	TA=125°C – Vbias	77x3 Lot	Parameter deviation within spec. limits at 1000h	No parameter deviation out of spec. limits at 1000 hours
PRESSURE POT	<i>D.U.T. PRECONDITIONED</i> TA=121°C – PA=2ATM	77x3 Lot	Parameter deviation within spec. limits at 168h	No parameter deviation out of spec. limits at 168 hours
THERMAL CYCLES AIR TO AIR	<i>D.U.T. PRECONDITIONED</i> TA=-65°C TO 150°C 1 HOUR/CYCLE	77x3 Lot	Parameter deviation within spec. limits at 500cycles	No parameter deviation out of spec. limits at 500 cycles
SMD MOISTURE INDUCED STRESS	DRYNG 24H @ 125°C STORE 192H @ TA=30°C RH=60% IR 3 times @ Tmax= 260°C	25x3 Lot	Parameter deviation within spec. limits at end of test	No parameter deviation out of spec. limits at end of test

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## 4 Annexes

### 4.1 Tests Description

Test name	Description	Purpose
<b>Die Oriented</b>		
<b>HTB</b> High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
<b>Package Oriented</b>		
<b>AC autoclave</b>	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
<b>TC Temperature Cycling</b>	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
<b>THB Temperature Humidity Bias</b>	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

## 5 GLOSSARY

<b>ESD</b>	Electro Static Discharge
<b>ELFR</b>	Early Life Failure Rate
<b>GL</b>	Gate Leakage
<b>HTB</b>	High Temperature Bias
<b>HTRB</b>	High Temperature Reverse Bias
<b>HTS</b>	High Temperature Storage
<b>T.H.B.</b>	Temperature Humidity Bias
<b>T.C.</b>	Thermal Cycle
<b>P.P.</b>	Pressure Pot
<b>P.C.</b>	Preconditioning

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